SPECIFICATION

TITLE OF THE INVENTION

5   PROCESS FOR MANUFACTURING A SEMICONDUCTOR WAFER,

A SEMICONDUCTOR WAFER, PROCESS FOR MANUFACTURING

A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

10   BACKGROUND OF THE INVENTION

The present invention relates to a process for

manufacturing a semiconductor wafer, a semiconductor

wafer, a process for manufacturing a semiconductor

integrated circuit device, and a semiconductor

15   integrated circuit device and, more particularly, to a

technique which is effective if applied to the

so-called "epitaxial wafer manufacturing process" for

forming an epitaxial layer over the surface of a

semiconductor substrate body, an epitaxial wafer, a

20   process for manufacturing a semiconductor integrated

circuit device by using the epitaxial wafer, and a

semiconductor integrated circuit device.

The epitaxial wafer is a semiconductor wafer

which is formed with an epitaxial layer over the

25   principal surface of a mirror-finished (or -polished)

semiconductor mirror wafer (or polished wafer) by the epitaxial growth method. Incidentally, the epitaxial growth method is described, for example, on pp. 51 to 74 of "VLSI TECHNOLOGY", edited by S. M. Sze and issued in 1983 by McGraw-Hill. On the other hand, the polishing is described on pp. 39 to 42 of the same Publication, for example.

The epitaxial wafer is featured in that it is excellent in suppressing the soft errors and resisting to the latchup, and in that the gate insulating film to be formed over the epitaxial layer can have excellent breakdown characteristics to drastically reduce the defect density of the gate insulating film. Thus, there has been promoted the application of the epitaxial wafer to the technique for manufacturing the semiconductor integrated circuit device.

As to this epitaxial wafer, there are the following two techniques.

The first technique is described on pp. 761 to 763 of "Applied Physics, Vol. 60, No. 8", issued on August 10, 1991 by Japanese Association of Applied Physics. There is described an epitaxial wafer, in which a p^+-type (or n^+-type) semiconductor substrate is formed thereover with a p- (or n-) type epitaxial layer containing a p- (or n-) type impurity having a

lower concentration than the p- (or n-) type impurity
concentration of the semiconductor substrate.

In this case, there is described the structure in
which a semiconductor region called the "well" is
5   formed in the epitaxial layer and is formed thereover
with a MOS. FET. Since the well of this case is formed
by the diffusion of the impurity from the surface of
the epitaxial layer, the impurity concentration in the
well is distributed to be high in the surface and low
10   in its inside.

The second technique is described in Japanese
Patent Laid-Open No. 260832/1989, for example and is
directed to an epitaxial wafer which has a p-type
epitaxial layer over a p-type semiconductor substrate.
15   In this case, an element forming diffusion layer is
formed to extend from the surface of the epitaxial
layer to the upper portion of the semiconductor
substrate.

Also described is a process, in which the
20   semiconductor substrate body is doped at the time of
forming the diffusion layer with a diffusion layer
forming impurity so that simultaneously with the
growth of the epitaxial layer over the semiconductor
substrate body, the impurity in the upper portion of
25   the semiconductor substrate body may be diffused to

form the diffusion layer.

The distribution of the impurity concentration of this case is made to have such a plateau curve having a peak at the boundary between the epitaxial layer and the semiconductor substrate body that the impurity concentration is low at the surface side of the epitaxial layer, high at the boundary between the epitaxial layer and the semiconductor substrate body and low in the semiconductor substrate body.

SUMMARY OF THE INVENTION

However, the semiconductor integrated circuit device manufactured according to the aforementioned first technique is excellent in the performance and reliability but has a problem in the cost because the semiconductor substrate used contains a (p$^+$-type or n$^+$-type) impurity in a high concentration and is expensive and because an epitaxial layer having a large thickness is formed over the semiconductor substrate.

According to the aforementioned second technique, on the other hand, the diffusion layer is formed by the so-called "upper diffusion" to diffuse the impurity in the upper portion of the semiconductor substrate. As a result, the impurity concentration is

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so difficult to set that there arise a problem that the diffusion layer forming accuracy drops. Another problem is that it is obliged to change the LSI (i.e., Large Scale Integration circuit) manufacturing process

5   using the so-called "mirror wafer".

An object of the present invention is to provide a technique capable of the cost for a semiconductor wafer having a semiconductor single crystal layer over a semiconductor substrate.

10   Another object of the present invention is to provide a technique capable of improving the performance and reliability of a semiconductor integrated circuit device and reducing the cost for the semiconductor integrated circuit device.

15   An object of the present invention is to provide a technique capable of facilitating the control of forming a semiconductor region on the semiconductor wafer which has the semiconductor single crystal layer over the semiconductor substrate.

20   An object of the present invention is to provide a technique capable of using a process for manufacturing the semiconductor integrated circuit device using the so-called "mirror wafer", as it is.

The aforementioned and other objects and the

25   novel features of the present invention will become

apparent from the following description to be made
with reference to the accompanying drawings.

Representatives of the invention disclosed herein
will be briefly described in the following.

5   Specifically, according to the present invention,
there is provided a process for manufacturing a
semiconductor wafer, comprising the step of forming
such a semiconductor single crystal layer over the
surface of a relatively lightly doped semiconductor

10   substrate body, which contains an impurity of a
predetermined conduction type, as contains an impurity
having the same conduction type as that of said
impurity and the same concentration as the designed
one of said impurity.

15   Moreover, according to the present invention,
there is provided a process for manufacturing a
semiconductor integrated circuit device, comprising:
the step of preparing a relatively lightly doped
semiconductor substrate body, which contains an

20   impurity of a predetermined conduction type and which
is formed over the surface of a semiconductor single
crystal layer containing an impurity having the same
conduction type as that of said impurity and the same
concentration as the designed one of said impurity;

25   and the step of forming an oxide film over said

semiconductor single crystal layer.

Moreover, according to the present invention, there is provided a process for manufacturing a

5 semiconductor integrated circuit device, comprising: the step of preparing a relatively lightly doped semiconductor substrate body, which contains an impurity of a predetermined conduction type and which is formed over the surface of a semiconductor single

10 crystal layer containing an impurity having the same conduction type as that of said impurity and a concentration not higher than that of said semiconductor substrate body; the step of forming a first semiconductor region extending from the surface

15 of said semiconductor single crystal layer to the upper portion of said semiconductor substrate body and having the same conduction type as that of said impurity and its impurity concentration gradually lowered depthwise of said semiconductor single crystal

20 layer; and the step of forming an oxide film over said semiconductor region.

Moreover, according to the present invention, there is provided a semiconductor integrated circuit device manufacturing method comprising the step of

25 doping said semiconductor single crystal layer with

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the ions an impurity and then thermally diffusing said impurity, at the step of forming said first semiconductor region.

5   Moreover, according to the present invention, there is provided a semiconductor integrated circuit device manufacturing method characterized in that said first semiconductor region is a well to be used for forming a complementary MOS·FET

10   (Metal-Oxide-Semiconductor·Field-Effect-Transistor) circuit (i.e., for forming a complementary MIS (Metal-Insulator-Semiconductor)·FET circuit).

According to the aforementioned semiconductor wafer manufacturing process of the present invention,

15   any semiconductor substrate body of high price and density (of p⁺- or n⁺-type) need not be used, and the semiconductor single crystal layer can be thinned, so that the cost for the semiconductor wafer capable of realizing high element characteristics and reliability

20   can be lowered.

According to the aforementioned semiconductor integrated circuit device manufacturing process of the present invention, moreover, a gate insulating film having an excellent film quality can be formed by

25   forming the gate insulating film of a MOS·FET over a

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semiconductor single crystal layer so that the gate

insulating film can have its breakdown voltage raised

to reduce the defect density of the gate insulating

film. Moreover, the semiconductor substrate body of

5   high price and density need not be used, but the

semiconductor single crystal layer can be thinned to

reduce the cost for the semiconductor integrated

circuit device having high element characteristics and

reliability.

10   According to the aforementioned semiconductor

integrated circuit device manufacturing process of the

present invention, moreover, the degree of freedom for

setting the impurity concentration and depth is so

high when a semiconductor region such as a well is

15   formed in the semiconductor substrate, as to

facilitate the control of the formation. As a result,

it is possible to reduce the defective products

thereby to improve the production yield. Moreover,

the cost for the semiconductor integrated circuit

20   device can be lowered.

According to the aforementioned semiconductor

integrated circuit device manufacturing process of the

present invention, moreover, the impurity

concentration of the semiconductor substrate body

25   below the semiconductor single crystal layer is made

higher than that of the semiconductor single crystal layer, so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup.

5

According to the aforementioned semiconductor integrated circuit device manufacturing process of the present invention, moreover, since the first semiconductor region is formed by the ion implantation method and the thermal diffusion method, the

10 semiconductor integrated circuit device can be manufactured without being accompanied by any change in the design or manufacture process but by using the same method as that of the semiconductor integrated

15 circuit device having the so-called "mirror wafer", when it is to be manufactured by using the semiconductor wafer having the semiconductor single crystal layer over the semiconductor substrate body.

According to the aforementioned semiconductor

20 integrated circuit device manufacturing process of the present invention, moreover, since the memory cell of the dynamic type random access memory is formed over the semiconductor single crystal layer having less defects such as the precipitation of oxygen, it is

25 possible to reduce the junction leakage current in the

source region and the drain region of the transfer MOS
·FET of the memory cell. Since, moreover, the charge
leakage in the capacitor of the memory cell can be
suppressed to elongate the charge storage time period,

5   it is possible to improve the refresh characteristics.
As a result, it is possible to improve the
performance, reliability and production yield of the
dynamic type random access memory.

According to the aforementioned semiconductor

10   integrated circuit device manufacturing process of the
present invention, moreover, since the memory cell of
the static type random access memory is formed over
the semiconductor single crystal layer having less
defects such as the precipitation of oxygen, the

15   junction leakage current of the source region and
drain region of the MOS. FET composing the memory cell
can be reduced to improve the data retention level
thereby to reduce the data retention fault percentage.
As a result, it is possible to improve the

20   performance, reliability and production yield of the
static type random access memory.

According to the aforementioned semiconductor
integrated circuit device manufacturing process of the
present invention, moreover, the memory cell of a read

25   only memory capable of electrically erasing and

programming data is formed over the semiconductor

single crystal layer having less defects such as the

precipitation of oxygen, so that the resistance to the

data programming can be improved and so that the

5   dispersion of the data erasure can be reduced. As a

result, it is possible to improve the performance,

reliability and production yield of the read only

memory capable of electrically erasing and programming

the data.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a section showing an essential portion

of a semiconductor integrated circuit device according

to one embodiment of the present invention;

15   Fig. 2 is a top plan view showing a semiconductor

wafer to be used at a step of manufacturing the

semiconductor integrated circuit device of Fig. 1;

Fig. 3 is a section showing an essential portion

at a step of manufacturing the semiconductor

20   integrated circuit device of Fig. 1;

Fig. 4 is a section showing an essential portion

at the step, as subsequent to Fig. 3, of manufacturing

the semiconductor integrated circuit device of Fig. 1;

Fig. 5 is a section showing an essential portion

25   at the step, as subsequent to Fig. 4, of manufacturing

the semiconductor integrated circuit device of Fig. 1;

Fig. 6 is a section showing an essential portion at the step, as subsequent to Fig. 5, of manufacturing the semiconductor integrated circuit device of Fig. 1;

5   Fig. 7 is a section showing an essential portion at the step, as subsequent to Fig. 6, of manufacturing the semiconductor integrated circuit device of Fig. 1;

Fig. 8 is a section showing an essential portion at the step, as subsequent to Fig. 7, of manufacturing

10   the semiconductor integrated circuit device of Fig. 1;

Fig. 9 is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention;

Fig. 10 is a section showing an essential portion

15   at a step of manufacturing the semiconductor integrated circuit device of Fig. 9;

Fig. 11 is a section showing an essential portion at the step, as subsequent to Fig. 10, of manufacturing the semiconductor integrated circuit

20   device of Fig. 9;

Fig. 12 is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention;

Fig. 13 is a section showing an essential portion

25   at a step of manufacturing the semiconductor

integrated circuit device of Fig. 12;

Fig. 14 is a section showing an essential portion at the step, as subsequent to Fig. 13, of manufacturing the semiconductor integrated circuit device of Fig. 12;

Fig. 15 is a section showing an essential portion at the step, as subsequent to Fig. 14, of manufacturing the semiconductor integrated circuit device of Fig. 12;

Fig. 16 is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention;

Fig. 17 is an impurity distribution diagram in the semiconductor integrated circuit device of Fig. 16 and has an abscissa indicating the depth from the surface of an epitaxial layer 2E and an ordinate indicating an impurity concentration;

Fig. 18 is an impurity distribution diagram in the semiconductor integrated circuit device, as has been described in the prior art and has an abscissa indicating the depth from the surface of an epitaxial layer EP1 and an ordinate indicating an impurity concentration;

Fig. 19 is an impurity distribution diagram in the semiconductor integrated circuit device, as has

been described in the prior art and has an abscissa
indicating the depth from the surface of an epitaxial
layer EP2 and an ordinate indicating an impurity
concentration;

5   Fig. 20 is a section showing an essential portion
of a semiconductor substrate at a step of
manufacturing the semiconductor integrated circuit
device of Fig. 16;

      Fig. 21 is a section showing an essential portion
10   of the semiconductor substrate at the step, as
subsequent to Fig. 20, of manufacturing the
semiconductor integrated circuit device of Fig. 16;

      Fig. 22 is a section showing an essential portion
of the semiconductor substrate at the step, as
15   subsequent to Fig. 21, of manufacturing the
semiconductor integrated circuit device of Fig. 16;

      Fig. 23 is a section showing an essential portion
of the semiconductor substrate at the step, as
subsequent to Fig. 22, of manufacturing the
20   semiconductor integrated circuit device of Fig. 16;

      Fig. 24 is a section showing an essential portion
of the semiconductor substrate at the step, as
subsequent to Fig. 23, of manufacturing the
semiconductor integrated circuit device of Fig. 16;

25   Fig. 25 is a graph diagram for explaining the

effects of the semiconductor integrated circuit device of the present embodiment;

Fig. 26(A) is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention;

Fig. 26(B) is a circuit diagram showing a memory cell of the semiconductor integrated circuit device of Fig. 26(A);

Fig. 27(A) is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention;

Fig. 27(B) is a circuit diagram showing a memory cell of the semiconductor integrated circuit device of Fig. 27(A);

Fig. 28 is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention;

Fig. 29 is a section showing an essential portion at a step of manufacturing a semiconductor integrated circuit device according to another embodiment of the present invention; and

Fig. 30 is a section showing an essential portion at the step, as subsequent to Fig. 29, of

manufacturing a semiconductor integrated circuit

device according to another embodiment of the present

invention.

5   DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will be described in detail

in the following in connection with its embodiments

with reference to the accompanying drawings.

(Embodiment 1)

10   Fig. 1 is a section showing an essential portion

of a semiconductor integrated circuit device according

to one embodiment of the present invention; Fig. 2 is

a top plan view of a semiconductor wafer to be used in

a process for manufacturing the semiconductor

15   integrated circuit device of Fig. 1; and Figs. 3 to 8

are sections showing an essential portion in a process

for manufacturing the semiconductor integrated circuit

device of Fig. 1.

As shown in Fig. 1, a semiconductor substrate 2

20   constituting a semiconductor integrated circuit device

1 of the present embodiment 1 is constructed of a

semiconductor substrate body 2S, an epitaxial layer

(i.e., semiconductor single crystal layer) 2E and a

gettering layer (i.e., trap region) 2B.

25   Incidentally, the gettering layer is described,

for example, on pp. 42 to 44 of "VLSI TECHNOLOGY",

edited by S. M. Sze and issued in 1983 by McGraw-Hill.

The semiconductor substrate body 2S is made of a

single crystal of p$^-$-type silicon (Si) having a

5   thickness of about 500 to 800 µm, for example. The

semiconductor substrate body 2S is doped with a p-type

impurity such as boron (B) in a concentration of about

1.3 x 10^{15} atoms/cm^3.

Over the principal surface of the semiconductor

10   substrate body 2S, there is formed the epitaxial layer

2E which is made of a single crystal of p$^-$-type Si, for

example. This epitaxial layer 2E is doped with a

p-type impurity such as boron in a concentration equal

to the designed one of the semiconductor substrate

15   body 2S, e.g., 1.3 x 10^{15} atoms/cm^3.

Here, the designed impurity concentration is

intended to cover an allowable value. Specifically,

the equality to the designed impurity concentration

means that, in case the semiconductor substrate body

20   2S has its designed impurity concentration expressed

by [impurity concentration: A] ± [allowable value: α]

and has an actual impurity concentration of A, the

semiconductor substrate body 2S and the epitaxial

layer 2E have equal impurity concentrations if the

25   actual impurity concentration of the epitaxial layer

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2E is not at A but within A ± α.

Thus, in the present embodiment 1, the p⁻-type epitaxial layer 2E is formed over the relatively lightly doped p⁻-type semiconductor substrate body 2S, 5 and any precious heavily doped p⁺-type semiconductor substrate body is not used so that the cost for the semiconductor substrate 2 can be reduced to one half or so.

In case the cost for the semiconductor substrate 10 of the prior art having the p⁻-type epitaxial layer formed over the p⁺-type semiconductor substrate body, for example, is 2.5 to 3 times as high as that of the ordinary semiconductor substrate having no epitaxial layer. On the contrary, the cost for the 15 semiconductor substrate of the present embodiment 1 can be suppressed within 1.5 times as high as that of the ordinary semiconductor substrate. As a result, the cost for the semiconductor integrated circuit device can be lowered.

20 The epitaxial layer 2E is made relatively thin to have a thickness of about 1 µm. As a result, the following effects can be attained.

At first, it is easy to control the setting of the thickness or resistivity of the epitaxial layer 25 2E. Secondly, for the first reason, the filming

apparatus for forming the epitaxial layer is not

required to have a high filming accuracy so that it

need not be expensive. Thirdly, the epitaxial layer

can be easily formed to improve the throughput.

5   Fourthly, for the first, second and third reasons, it

is possible to reduce the cost for the semiconductor

substrate 2.

The lower limit of the thickness of the epitaxial

layer 2E is one half or more of the thickness of the

10   gate insulating film in the later-described MOS·FET.

This setting is made while considering that one half

of the thickness of the gate insulating film of the

MOS·FET goes into the side of the semiconductor

substrate 2 when the gate insulating film is formed.

15   Specifically, in case the epitaxial layer 2E is

made thinner than one half of the thickness of a gate

insulating film, its entirety is covered with the gate

insulating film when this film is to be formed over

the epitaxial layer 2E. As a result, the structure is

20   made such that the gate insulating film is formed over

the semiconductor substrate body 2S. This structure

loses the effect of the case, in which the gate

insulating film is formed over the epitaxial layer 2E,

namely, that an excellent gate insulating film can be

25   formed to improve its breakdown voltage.

Incidentally, the lower limit of the thickness of the epitaxial layer 2E is frequently set to 0.3 μm by evaluating the performance of the gate insulating film (e.g., the gate breakdown voltage), as will be

5   described with reference to Fig. 25.

On the other hand, the upper limit of the thickness of the epitaxial layer 2E cannot be generally said because it depends upon the product or manufacturing conditions, but may desirably be less

10   than 5 μm, for example, if the following is considered.

Specifically, first of all, the upper surface of the epitaxial layer 2E can retain flatness. If the epitaxial layer 2E is made thicker, the level

15   difference of the principal surface of the semiconductor substrate body 2S is accordingly increased, but no substantial difference is caused by the thickness of such extent.

If the principal surface has an excessively large

20   roughness, a larger level difference than the focal depth may be made in a photolithography for the later-described MIS device forming step, thus causing a problem that the pattern cannot be formed by the photolithography.

25   Secondly, the cost for the mother material of the

semiconductor substrate 2 or the semiconductor wafer

(i.e., the later-described epitaxial wafer) can be

suppressed within a low price. If the epitaxial layer

2E is thickened, it is difficult to control the

5   filming operation, as described above, so that the

cost for the semiconductor wafer (i.e., the

later-described epitaxial wafer) rises. However, this

thickness will not invite a drastic increase in the

cost.

10   Thirdly, the roughness, if any, on the principal

surface of the semiconductor substrate body 2S can be

ignored. With the thickness of this order, the

roughness will not make a large level difference.

Fourthly, when the epitaxial layer is to be

15   formed over the semiconductor wafer (i.e., the later-

described mirror wafer), it is possible to prevent any

roughness (i.e., crown) from being formed in the

vicinity of the outer circumference of the principal

surface of the semiconductor wafer (i.e., the later-

20   described mirror wafer). In case a thick epitaxial

layer is to be formed over the semiconductor wafer

(i.e., the later-described mirror wafer), the

roughness called the crown will be formed in the

vicinity of the outer periphery of the principal

25   surface of the semiconductor wafer (i.e., the

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later-described mirror wafer). With the thickness of that order, the roughness is not formed (or can be ignored).

Considering the aforementioned points, the thickness of the epitaxial layer 2E is preferred to range from 0.3 μm to 5 μm. However, the range of 0.3 μm to 3 μm is frequently employed, and the optimum range is from 0.3 μm to 1.0 μm.

Over the principal surface of the epitaxial layer 2E, there is formed a field insulating film 3 which is made of silicon dioxide (SiO_2), for example. Incidentally, a channel stopper region is formed below the field insulating film 3, although not shown.

The element forming region, as enclosed by the field insulating film 3, is formed, for example, with an n-channel MOS·FET (as will be shortly referred to as "nMOS") 4N and a p-channel MOS. FET (as will be shortly referred to as "pMOS") 4P, and these nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit. Incidentally, the following description is directed to the MOS·FET, but the present invention may naturally be modified by a MIS·FET.

In the present embodiment 1, however, both the nMOS 4N and the pMOS 4P are given an ordinary MOS·FET

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structure but should not be limited thereto and may be

made of MOS·FETs having the LDD (i.e., Lightly Doped

Drain) structure.

The nMOS 4N has the following components.

5   Specifically, the nMOS 4N is composed of: a pair of

semiconductor regions 4Na and 4Nb formed over the

epitaxial layer 2E and apart from each other; a gate

insulating film 4Nc formed over the epitaxial layer

2E; and a gate electrode 4Nd formed over the gate

10   insulating film 4Nc.

The semiconductor regions 4Na and 4Nb are regions

for forming the source-drain regions of the nMOS 4N.

The semiconductor regions 4Na and 4Nb are doped with

an n-type impurity such as phosphor (P) or arsenic

15   (As) in a concentration (dose) of about 1×10^{15}

atoms/cm^2. The semiconductor regions 4Na and 4Nb are

made as deep as about 0.5 µm and formed in the range

of the thickness of the epitaxial layer 2E.

The gate insulating film 4Nc is made of SiO_2

20   having a thickness of about 18 nm, for example, and

formed over the epitaxial layer 2E. As a result, the

following effects can be achieved.

First of all, by forming the gate insulating film

4Nc of the MOS·FET over the semiconductor single

25   crystal layer 2E formed of the epitaxial layer 2E, the

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gate insulating film 4Nc having an excellent film quality can be formed, as described above, to improve its breakdown voltage. Secondly, the defect density (i.e., the number of defects to be caused within a

5   predetermined range) of the gate insulating film 4Nc can be improved (reduced) by one figure or more.

The gate electrode 4Nd is made of a single layer film of poly-silicon having a low resistance, for example. Here, the gate electrode 4Nd is not limited

10   to the single layer film of poly-silicon of low resistance but can be modified in various manners. For example, the gate electrode 4Nd may be constructed by laminating a silicide film of tungsten silicide (WSi_2) over the poly-silicon film of low resistance.

15   Incidentally, a semiconductor region 5Sa formed over the epitaxial layer 2E is a region for setting the substrate potential at the side of the nMOS 4N. This semiconductor region 5Sa is doped with a p-type impurity such as boron in a concentration (. dose) of

20   about 1×10^{15} atoms/cm^2.

On the other hand, the nMOS 4P is formed in an n-well 6 which is formed over the semiconductor substrate 2. The n-well 6 is doped with an n-type impurity such as phosphor or arsenic in a

25   concentration (dose) of 1×10^{13} atoms/cm^2. The

n-well 6 is as deep as about 1.5 ~ 4 μm and extends deeper than the epitaxial layer 2E. Specifically, the n-well 6 is formed in the epitaxial layer 2E and the semiconductor substrate body 2S to have a larger depth than the film thickness of the epitaxial layer 2E.

The pMOS 4P has the following components. Specifically, the pMOS 4P is composed of: a pair of semiconductor regions 4Pa and 4Pb formed over the epitaxial layer 2E and apart from each other; a gate insulating film 4Pc formed over the epitaxial layer 2E; and a gate electrode 4Pd formed over the gate insulating film 4Pc.

The semiconductor regions 4Pa and 4Pb are regions for forming the source-drain regions of the pMOS 4P. The semiconductor regions 4Pa and 4Pb are doped with an p-type impurity such as boron in a concentration (dose) of about 1×10^{18} atoms/cm^2. The semiconductor regions 4Pa and 4Pb are made as deep as about 0.5 μm and formed in the range of the thickness of the epitaxial layer 2E.

The gate insulating film 4Pc is made of SiO$_2$ having a thickness of about 18 nm, for example, and formed over the epitaxial layer 2E. As a result, the same effects as those of the pMOS 4N can be achieved.

First of all, the gate insulating film 4Pc having

an excellent film quality can be formed, to improve

its breakdown voltage. Secondly, the defect density

of the gate insulating film 4Pc can be improved (or

reduced) by one figure or more.

5   The gate electrode 4Pd is made of a single layer

film of poly-silicon having a low resistance, for

example. Here, the gate electrode 4Pd is not limited

to the single layer film of poly-silicon of low

resistance but can be modified in various manners.

10   For example, the gate electrode 4Pd may be constructed

by laminating a silicide film of WSi_2 over the poly-

silicon film of low resistance.

     Incidentally, a semiconductor region 5Sb formed

over the epitaxial layer 2E is a region for setting

15   the substrate potential at the side of the pMOS 4P.

This semiconductor region 5Sb is doped with an n-type

impurity such as phosphor or arsenic in a

concentration (dose) of about 1 x 10^{18} atoms/cm^2.

     On the semiconductor substrate 2, there is

20   deposited an insulating film 7 which is made of SiO_2,

for example. This insulating film 7 is formed in

predetermined positions with connection holes 8 for

exposing the semiconductor regions 4Na and 4Nb of the

nMOS 4N, the semiconductor regions 4Pa and 4Pb of the

25   pMOS 4P, and the semiconductor regions 5Sa and 5Sb for

the substrate potential to the outside.

The semiconductor regions 4Na and 4Nb of the aforementioned nMOS 4N are electrically connected with electrodes 9Na and 9Nb, respectively, through the connection holes 8. On the other hand, the semiconductor regions 4Pa and 4Pb of the pMOS 4P are electrically connected with electrodes 9Pa and 9Pb, respectively, through the electrodes 8. Moreover, the semiconductor region 4Nb of the nMOS 4N is electrically connected with the semiconductor region 4Pb of the pMOS 4P through a first-layer wiring line 10 connecting the electrodes 9Nb and 9Pb.

On the other hand, the semiconductor regions 5Sa and 5Sb for the substrate potential are electrically connected with electrodes 9Sa and 9Sb, respectively, through the connection holes 8.

Those electrodes 9Na, 9Nb, 9Pa, 9Pb, 9Sa and 9Sb and first-layer wiring line 10 are made of an alloy of aluminum (A$\underline{l}$)-Si-Copper (Cu), for example.

On the insulating film 7, there is deposited a surface protecting film 11 which is formed by laminating a SiO_2 film and a silicon carbide (Si_3N_4) sequentially from the lower layer, for example. The surface protecting film 11 covers the electrodes 9Na, 9Nb, 9Pa, 9Pb, 9Sa and 9Sb and the first-layer wiring

line 10.

On the other hand, the semiconductor substrate 2 is formed on its back with a gettering layer 2G. This gettering layer 2G is a functional layer for trapping a heavy metal element such as iron (Fe), nickel (Ni), Cu or chromium (Cr) and is formed by covering the back of the semiconductor substrate 2 with a semiconductor film of poly-silicon, for example.

With reference to Figs. 1 to 8, here will be described a process for manufacturing a semiconductor integrated circuit device according to the present embodiment 1.

First of all, a (not-shown) column-shaped p^--type Si single crystal having a crystal face of <100> azimuth is prepared by the Czochralski method. The impurity to be used is exemplified by a p-type impurity such as boron in a concentration of about 1.3 $\times$ 10^{15} atoms/cm^3.

Subsequently, the column-shaped p^--type Si single crystal cut into slices, and these slices are subjected, if desired, to a chamfering treatment, a surface cleaning treatment such as a chemical etching treatment, and a working strain removing treatment. After this, the slices have their principal surfaces mirror-polished by the chemical-mechanical polishing

method or the like to prepare a mirror wafer 2W, as shown in Figs. 2 and 3. Incidentally, the mirror wafer 2W is the mother material of the aforementioned semiconductor substrate body 2S.

5   Next, the poly-silicon is deposited on the back of the mirror wafer 2W, as shown in Fig. 4, by the CVD (i.e., Chemical Vapor Deposition) method to form the gettering layer 2G. This gettering layer 2G is a functional layer for trapping a heavy metal element.

10   Subsequently, the epitaxial layer 2E, which is made of a p^--type Si single crystal as thin as about 1 μm, is formed over the principal surface (as located at the mirror surface side) of the mirror wafer 2W by the CVD method (e.g., the epitaxial growth method) of

15   about 980°C, for example, by using monosilane (SiH_4) gas and hydrogen (H_2) gas, thereby to manufacture an epitaxial wafer (or semiconductor wafer) 2WE.

At this time, the impurity concentration in the epitaxial layer 2E is set equal to the designed one of

20   the mirror wafer 2W. The epitaxial layer 2E is doped with a p-type impurity such as boron in a concentration of about 1.3×10^{15} atoms/cm^3.

After this, the not-shown ion implantation mask is formed over the epitaxial wafer 2WE and is then

25   used to dope a predetermined position of the epitaxial

wafer 2WE, as shown in Fig. 5, with an n-type impurity

such as phosphor or arsenic by the ion implantation

method. After this, the epitaxial wafer 2WE is

subjected to a heat treatment to form the n-well 6.

5   An ion implantation impurity concentration

(dose) for forming that n-well 6 is at about 1 x 10^{13}

atoms/cm^2 and is as deep as about 1.5 to 4 µm and

deeper than the epitaxial layer 2E.

        Next, as shown in Fig. 6, the field insulating

10   film 3 made of SiO_2 or the like is formed over the

principal surface of the epitaxial layer 2E by the

LOCOS method or the like. After this, the element

forming region, as enclosed by the field insulating

film 3, is simultaneously formed with the gate

15   insulating films 4Nc and 4Pc made of SiO_2 or the like

having a thickness of about 180 angstroms by the

thermal oxidation method or the like.

        In the present embodiment 1, the gate insulating

films 4Nc and 4Pc can be formed to have an excellent

20   film quality by forming them over the epitaxial layer

2E so that their breakdown voltages can be improved.

Moreover, the gate insulating films 4Nc and 4Pc can

have their defect densities improved by one figure or

more.

25   Subsequently, as shown in Fig. 7, the gate

insulating films 4Nd and 4Pd of poly-silicon having a low resistance are simultaneously formed over the gate insulating films 4Nc and 4Pc. After this, the gate insulating films 4Nd and 4Pd are used as masks to form

5   the paired gate insulating films 4Na and 4Nb and the paired gate insulating films 4Pa and 4Pb by different ion implantation steps, to form the nMOS 4n and pMOS 4P over the epitaxial wafer 2WE.

After this, the semiconductor regions 5Sa and 5Sb

10   are separately formed in predetermined positions of the epitaxial layer 2E. After this, as shown in Fig. 8, the insulating film 7 made of SiO_2, for example, is deposited over the epitaxial wafer 2WE by the CVD method or the like.

15   Next, the insulating film 7 is formed with the connection holes 8 to expose the semiconductor regions 4Na and 4Nb of the nMOS 4N, the semiconductor regions 4Pa and 4Pb of the pMOS 4P and the semiconductor regions 5SA and 5Sb for the substrate potential to the

20   outside. After this, a conductor film 9 made of the Al-Si-Cu alloy, for example, is deposited over the epitaxial wafer 2WE by the sputtering method or the evaporation method.

Subsequently, the conductor film 9 is patterned

25   by the dry etching method or the like to

simultaneously form the electrodes 9Na, 9Nb, 9Pa, 9Pb,
9Sa and 9Sb and the first wiring line 10, as shown in
Fig. 1.

After this, the surface protecting film 11 is

5   formed over the epitaxial wafer 2WE by sequentially
depositing the insulating film of SiO_2 and the
insulating film of Si_3N_4, for example, by the CVD
method or the like. After this, the epitaxial wafer
2WE is divided into individual semiconductor chips to

10   manufacture the semiconductor integrated circuit
device 1, as shown in Fig. 1.

Thus, according to the present embodiment 1, the
following effects can be achieved.

(1)   Since the gate insulating film 4Nc of the nMOS 4N

15   and the gate insulating film 4Pc of the pMOS 4P are
formed over the epitaxial layer 2E (or the
semiconductor single crystal layer), the gate
insulating films 4Nc and 4Pc having the excellent film
quality can be formed to improve their breakdown

20   voltages.

(2)   Thanks to the aforementioned effect (1), it is
possible to drastically reduce the defect densities of
the gate insulating films 4Nc and 4Pc.

(3)   Since the p⁻-type epitaxial layer 2E is formed

25   over the p⁻-type semiconductor substrate body 2S so

that any expensive heavily doped p⁺-type semiconductor substrate body is not used, the cost for the semiconductor substrate 2 (i.e., the epitaxial wafer 2WE) can be reduced to as low as one half.

5   (4)   Since the epitaxial layer 2E is made relatively thin, the control of setting of the thickness of the epitaxial layer 2E so that the filming apparatus for forming the epitaxial layer is neither required to have a high filming accuracy nor expensive. As a

10   result, it is possible to lower the cost for the semiconductor substrate 2 (i.e., the epitaxial wafer 2WE).

(5)   Thanks to the aforementioned effects (3) and (4), it is possible to lower the cost for the semiconductor

15   integrated circuit device.

(6)   Since the epitaxial layer 2E is made relatively thin, its upper surface can have its flatness retained.

(7)   Thanks to the aforementioned effects (1), (2) and

20   (6), it is possible to improve the performance, reliability and production yield of the semiconductor integrated circuit device.

(Embodiment 2)

Fig. 9 is a section showing an essential portion

25   of a semiconductor integrated circuit device according

to another embodiment of the present invention, and

Figs. 10 and 11 are sections showing an essential

portion at steps of manufacturing the semiconductor

integrated circuit device of Fig. 9.

5   The present embodiment 2 is different from the

embodiment 1 in that the semiconductor substrate body

2S is formed over its principal surface with a non-

defective layer 2A, which is formed thereover with the

epitaxial layer 2E.

10   The non-defective layer 2A is in the state having

substantially neither any structural defect (e.g., the

stacking fault or the dislocation loop) nor any

precipitation of oxygen, of which the former is

substantially zero whereas the latter is at about 0.1

15   cm^{-2}, when observed by the light scattering method.

For example, the non-defective layer 2A is made of a

p^{-}-type Si single crystal which have an impurity

content and a concentration equal to those of the

semiconductor substrate body 2S.

20   With reference to Figs. 9 to 11, here will be

described the process for manufacturing the

semiconductor integrated circuit device 1 of the

present embodiment 2.

First of all, as shown in Fig. 10, the mirror

25   wafer 2W is prepared as in the foregoing embodiment 1.

After this, the mirror wafer 2W is heated at a temperature (e.g., at about $1,100^\circ$C to $1,200^\circ$C for 10 to 60 minutes) in the H_2 gas atmosphere, for example, to form the non-defective layer 2A over the principal

5   surface of the mirror wafer 2W.

Subsequently, as shown in Fig. 11, poly-silicon, for example, is deposited on the back of the mirror wafer 2W by the CVD method or the like to form the gettering layer 2G. This gettering layer 2G is a

10 functional layer for trapping a heavy metal element.

After this, the epitaxial layer 2E made of a p^--type Si single crystal having a relatively small thickness of about 1 μm, for example, is formed over the non-defective layer 2A by the CVD method (e.g.,

15 the epitaxial growth method) using SiH_4 gas and H_2 gas, for example. At this time, the impurity and its concentration in the epitaxial layer 2E are similar to those of the foregoing embodiment 1. Moreover, the subsequent steps are similar to those of the

20 aforementioned embodiment 1, and their description will be omitted.

Thus, according to the present embodiment 2, the following effects can be achieved in addition to those obtained in the foregoing embodiment 1.

25 Specifically, since the non-detective layer 2A is

formed over the principal surface of the mirror wafer

2W prior to the formation of the epitaxial layer 2E,

the epitaxial layer 2E can be improved in its crystal

growth to reduce the defects and dislocations

5   drastically. As a result, it is possible to further

improve the production yield, performance and

reliability of the semiconductor integrated circuit

device.

(Embodiment 3)

10   Fig. 12 is a section showing an essential portion

of a semiconductor integrated circuit device according

to another embodiment of the present invention, and

Figs. 13 to 15 are sections showing an essential

portion in the steps of manufacturing the

15   semiconductor integrated circuit device of Fig. 12.

In the present embodiment 3, as will be described

later in connection with the forming method with

reference to Fig. 13, a p^+-type semiconductor region

(i.e., a heavily doped semiconductor region) 2B is

20   formed in a predetermined depth (of about 1 μm) of the

entire principal surface of the semiconductor

substrate body 2S. The p^+-type semiconductor region 2B

is doped with a p-type impurity such as boron in a

higher concentration of about 1×10^{18} atoms/cm^3 than

25   that of the epitaxial layer 2E or the semiconductor

substrate body 2S.

The p⁺-type semiconductor region 2B is a functional layer for suppressing the latchup of the CMOS circuit. Specifically, in the present embodiment

5   3, the p⁺-type semiconductor region 2B is formed so that the resistance of the surface layer side of the substrate can be drastically lowered to improve the resistance of the CMOS circuit to the latchup.

Moreover, the epitaxial layer 2E is thicker at

10 about 5 μm than those of the foregoing embodiments 1 and 2. The lower limit of the thickness of the epitaxial layer 2E is set to a deeper value than that of the n-well 6 in the pMOS forming region.

This is because the p⁺-type semiconductor region

15 2B is formed in the n-well 6 to make it difficult to set the impurity concentration in the n-well 6 if the thickness of the epitaxial layer 2E is made smaller than the depth of the n-well 6. On the other hand, the upper limit of the thickness of the epitaxial

20 layer 2E may desirably be less than 5 μm. This is reasoned as in the foregoing embodiment 1. However, the thickness may exceed that value so long as an increase in the cost is allowed.

With reference to Figs. 13 to 15, here will be

25 described the process for manufacturing such

semiconductor integrated circuit device 1.

First of all, as shown in Fig. 13, the mirror wafer 2W is prepared as in the foregoing embodiment 1. After this, the mirror wafer 2W (or the semiconductor substrate body 2S) is highly accurately doped with a p-type impurity such as boron to a predetermined depth (e.g., about 1 μm) from its principal surface. The impurity concentration at this time is about 1×10^{18} atoms/cm^3.

Subsequently, the mirror wafer 2W is thermally treated to form the p$^+$-type semiconductor region 2B. After this, a poly-silicon, for example, is deposited on the back of the mirror wafer 2W by the CVD method or the like to form the gettering layer 2G. This gettering layer 2G is a functional layer for trapping a heavy metal element.

After this, the epitaxial layer 2E (or the semiconductor single crystal layer) made of a p$^-$-type Si single crystal having a thickness of about 5 μm, for example, is formed over the principal surface (as located at the mirror surface side) of the mirror wafer 2W, as shown in Fig. 14, by the CVD method (i.e., the epitaxial growth method) using SiH$_4$ and H$_2$ gas, for example, to form the epitaxial wafer 2WE.

At this time, the impurity concentration in the

epitaxial layer 2E is set to be equal to the designed

one of the mirror wafer 2W. The epitaxial layer 2E is

doped with a p-type impurity such as boron, for

example, in a concentration of about 1.5 x 10^{15} atoms/

5   cm^3.

After this, the not-shown ion implantation mask

is formed over the epitaxial wafer 2WE and is then

used as a mask to dope a predetermined position of the

epitaxial wafer 2WE, as shown in Fig. 15, with an n-

10   type impurity such as phosphor or boron by the ion

implantation method. After this, the epitaxial wafer

2WE is subjected to a heat treatment to form the n-

well 6.

In the present embodiment 3, the n-well 6 has a

15   depth of about 3 μm and is formed in the epitaxial

layer 2E. The ion implantation impurity concentration

(dose) for forming that n-well 6 is at about 1 x

10^{13} atoms/cm^2. The subsequent steps are similar to

those of the aforementioned present embodiment 1 so

20   that their description will be omitted.

Thus, in the present embodiment 3, the following

effects can be achieved in addition to those of the

aforementioned embodiment 1.

Specifically, since the p⁺-type semiconductor

25   region 2B is formed in the p⁻-type semiconductor

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substrate body 2S, the resistance at the side of the

substrate surface can be drastically lowered to

improve the resistance of the CMOS circuit to the

latchup. As a result, it is possible to further

5 improve the performance, reliability and production

yield of the semiconductor integrated circuit device.

(Embodiment 4)

Fig. 16 is a section showing an essential portion

of a semiconductor integrated circuit device according

10 to another embodiment of the present invention; Fig.

17 is an impurity distribution diagram in the

semiconductor integrated circuit device of Fig. 16;

Figs. 18 and 19 are impurity distribution diagrams in

the semiconductor integrated circuit device having

15 been described in the prior art; Figs. 20 to 24 are

sections showing an essential portion in the steps of

manufacturing the semiconductor integrated circuit

device; and Fig. 25 is a graph for explaining the

effects of the semiconductor integrated circuit device

20 of the present embodiment. Incidentally, the portions

identical to those of the foregoing embodiment 1 are

designated at the common reference characters.

As shown in Fig. 16, the relatively lightly doped

semiconductor substrate body 2S constituting the

25 semiconductor integrated circuit device 1 of the

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present embodiment 4 is made of a p-type Si single

crystal or the like, for example. The semiconductor

substrate body 2S is doped with a p-type impurity such

as boron in a concentration of about 1.5 x 10^{15}

5   atoms/cm^3.

The semiconductor substrate body 2S is formed

over its principal surface with the epitaxial layer 2E

made of a p$^-$-type Si single crystal or the like. The

epitaxial layer 2E is doped with a p-type impurity

10   such as boron in a concentration lower than the

designed one of the semiconductor substrate body 2S.

Thus, in the present embodiment 4, the p$^-$-type

epitaxial layer 2E is formed over the p-type

semiconductor substrate body 2S as in the foregoing

15   embodiment 1 so that the expensive p$^+$-type

semiconductor substrate body need not be used to lower

the cost for the semiconductor substrate 2 to about

one half.

Since, moreover, the impurity concentration of

20   the semiconductor substrate body 2S is made higher

than that of the epitaxial layer 2E, the resistance of

the semiconductor substrate body 2S can be made lower

than that of the epitaxial layer 2E to improve the

resistance to the latchup.

25   As will be later shown in Fig. 17, the epitaxial

layer 2E has a thickness W_E (from the surface of the

epitaxial layer 2E) similar to that of the foregoing

embodiment 1, as exemplified by about 1 μm. As a

result, it is possible to achieve the same effects as

5   those described in connection with the foregoing

embodiment 1. The upper and lower limits of the

thickness of the epitaxial layer 2E are similar to

those of the foregoing embodiment 1.

The semiconductor substrate 2 is formed in its

10   upper portion with a p-well (i.e., the first

semiconductor region) 6p and an n-well (i.e., the

first semiconductor region) 6n. The p-well 6p is

doped with a p-type impurity such as boron. The

p-well 6p is formed with the nMOS 4N. On the other

15   hand, the n-well 6n is doped with an n-type impurity

such as phosphor. The n-well 6n is formed with the

pMOS 4P. As will be later shown in Fig. 17, the depth

W_W (i.e., the depth from the surface of the epitaxial

layer 2E) of the n-well 6n and the p-well 6p is larger

20   than the thickness W_E of the epitaxial layer 2E.

Incidentally, the CMOS circuit is constructed of

the nMOS 4N and the pMOS 4P, which have their

structures, materials and effects similar to those of

the foregoing embodiment 1. On the other hand, the

25   structures of the nMOS 4N and the pMOS 4P may be

changed to the double drain (or double diffused drain) structure and the LDD (i.e., Lightly Doped Drain) structure.

On the insulating film 7, there is deposited an insulating film 7a of SiO_2, for example, on which is deposited a flattening insulating film 7b. The insulating films 7, 7a and 7b are formed with connection holes 8a extending to reach the electrodes 9Nb and 9Pb, through which a second-layer wiring line 10a is electrically connected with the electrodes 9Na and 9Pa.

The second-layer wiring line 10a is formed by depositing a barrier layer 10a1 of titanium nitride (TiN), a conductor layer 10a2 of an Al-Si-Cu alloy and a barrier layer 10a3 of titanium nitride sequentially from the lower layer.

An insulating film 7c of SiO_2, for example, is deposited on the insulating film 7b to cover the second-layer wiring line 10a. On the insulating film 7c, there is deposited the surface protecting film 11. This surface protecting film 11 is formed by depositing an insulating film 11a of SiO_2 and an insulating film 11b of Si_3N_4, for example, sequentially from the lower layer.

Incidentally, in the present embodiment 4, the

aforementioned p-well 6p and n-well 6n are formed to

extend from the surface of the epitaxial layer 2E to

the upper portion of the semiconductor substrate body

2S, as shown in Figs. 16 and 17, and the p-well 6p and

5   n-well 6n have their impurity concentrations gradually

lowered in the depthwise direction from the principal

surface (having an impurity concentration N_w) of the

epitaxial layer 2E. Thus, the impurity concentration

of the p-well 6p is given such a gradient that it is

10   gradually lowered in the depthwise direction from the

surface of the epitaxial layer 2E, so that the

influence to be caused by the carriers (or electrons)

due to the α-ray is lowered. Specifically, the

electrons produced by the α-ray are attracted to the

15   substrate body 2S by that concentration gradient and

prevented from entering the p-well 6p so that the soft

errors can be reduced in case the MIS memory of the

DRAM or the like is formed in the p-well 6p. The

impurity concentration N_w in the principal surface of

20   the epitaxial layer 2E of the p-well 6p and the n-well

6n is at about 6×10^{16} atoms/cm^3, so that the impurity

concentration of the p-well 6p and the n-well 6n is at

5×10^{15} to 6×10^{16} atoms/cm^3.

In Fig. 17, letter A plots the impurity

25   concentration distributions of the epitaxial layer 2E

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and semiconductor substrate body 2S in the epitaxial

wafer state, and indicates that the impurity

concentration (N_E) of the epitaxial layer 2E is lower

than that (N_S) of the semiconductor substrate body 2S,

5   as described above. Thus, the p-well 6p is formed

after the p⁻- type epitaxial layer 2E is formed over

the p-type semiconductor substrate body 2S, the well

concentration (i.e., the concentration N_W of the well

surface) of the p-well 6p is not influenced by the

10   p-type impurity concentration of the semiconductor

substrate body 2S. Specifically, since the p⁻-type

epitaxial layer 2E is formed over the semiconductor

substrate body 2S, the well concentration N_W of the

p-well 6p is not influenced by the dispersion of the

15   p-type impurity concentration of the semiconductor

substrate body 2S so that the fluctuation of the Vth

of the MIS·FET is not caused by that dispersion. As a

result, the allowable concentration range can be

widened more than the prior art with respect to the

20   dispersion of the p-type impurity concentration of the

semiconductor substrate body 2S so that the cost for

the semiconductor integrated circuit device can be

lowered. In other words, in the prior art, only a

narrow range can be used as the p-type impurity

25   concentration of the semiconductor substrate body 2S

to raise the cost for the semiconductor integrated circuit device.

For comparisons, the impurity concentration distributions of the aforementioned two cases of the prior art are plotted in Figs. 18 and 19. Incidentally, Fig. 18 corresponds to the case of the aforementioned technique, as described on pp. 761 to 763 of "Applied Physics, Vol. 60, No. 8", issued on August 10, 1991, by Japanese Association of Applied Physics, and Fig. 19 corresponds to the case of the aforementioned technique, as described in the Japanese Patent Laid-Open No. 260832/1989.

In the technique shown in Fig. 18, the impurity concentration NS_1 of the semiconductor substrate body SB1 is higher than that of the epitaxial layer EP1. Moreover, the well WLL1 is formed in the epitaxial layer from the standpoint of setting the impurity concentration. This makes it necessary to make the epitaxial layer deeper, as at Wep1, than the well WLL1. In short, the thickness Wep1 of the epitaxial layer has to be larger than the depth of the well WLL1. Moreover, the well WLL1 of this case is formed by implanting the epitaxial layer EP1 with the impurity from the surface thereof, so that the impurity concentration is higher in the substrate

surface than in the inside.

In the technique shown in Fig. 19, the impurity
concentrations of both the semiconductor substrate
body SB2 and the epitaxial layer EP2 are set to be
5   low, as at NS_2. The well WLL2 is formed to extend
deeper, as at W_{w2}, than the depth Wep2 of the epitaxial
layer EP2. The well WLL2 of this case is formed by
the diffusion (i.e., the diffusion of the impurity of
the semiconductor substrate body SB2 from the
10   semiconductor substrate body to the epitaxial layer
EP2) at the time when the epitaxial layer EP2 is
formed over the semiconductor substrate body SB2 which
has been doped in its upper portion with a well
forming impurity. As a result, the impurity
15   concentration is low, as at NS_3, in the substrate
surface but high, as at NS_4, in the boundary region
between the epitaxial layer EP2 and the semiconductor
substrate body SB2 and gets lower internally of the
semiconductor substrate body.
20   With reference to Figs. 20 to 24, here will be
described the process for manufacturing the
semiconductor integrated circuit device of the present
embodiment 4.

First of all, as shown in Fig. 20, the mirror
25   wafer 2W or the mother material of the semiconductor

substrate body 2S made of a p-type Si single crystal

is formed over its mirror surface with the epitaxial

layer 2E, which is made of an Si single crystal having

the same conduction type as the mirror wafer 2W and

5 containing an impurity of a lower concentration than

that of the mirror wafer 2W, by the CVD method using

SiH_4 gas and H_2 gas similar to those of the foregoing

embodiment 1.

Here, the mirror wafer 2W has an impurity

10 concentration of about 1.5×10^{15} atoms/cm^3. Moreover,

the epitaxial layer 2E has a thickness W_E of about 1

µm, for example.

Subsequently, the mirror wafer 2W is formed in

its predetermined region with an insulating film 12a

15 made of SiO_z having a thickness of about 40 nm. After

this, a (not-shown) insulating film made of Si_3N_4

having a thickness of about 50 nm, for example, is

deposited on a predetermined region of the mirror

wafer 2W by the CVD method or the like.

20 After this, the film portion in the n-well

forming region is removed from the insulating film of

Si_3N_4 by the dry etching method or the like. After

this, the film portion and the resist film of the p-

well forming region in the insulating film of Si_3N_4 is

25 used as a mask to dope the exposed portion of the

epitaxial layer 2E with the ions of an n-type impurity

such as phosphor for forming the n-well. The ion

implanting energy at this time is at about 125 KeV,

and the dose is about 2 x 10^{13} atoms/cm^2.

5   After this, the film portion, as in the p-well

forming region, of the insulating film of Si_3N_4 is used

as a mask to form an insulating film 12b having a

thickness of about 120 nm over the epitaxial layer 2E

at the n-well side. After this, the insulating film

10   over the n-well forming region is used as an ion

implantation mask to dope the exposed portion of the

epitaxial layer 2E with a p-type impurity such as

boron for forming the p-well, for example. The ion

implantation energy at this time is about 60 KeV, and

15   the dose is about 8 x 10^{12} atoms/cm^2, for example.

      Next, the mirror wafer 2W is subjected to an

annealing treatment for extended diffusion for 3

hours, for example, to form the p-well 6p and the

n-well 6n having a depth of about 3 μm, for example.

20   The treatment temperature at this time is about

1,200°C, for example.

      In the present embodiment 4, at this annealing

treatment, the p-well 6p and the n-well 6n are

extended from the surface of the epitaxial layer 2E to

25   the upper portion of the mirror wafer 2W and made to

have their impurity concentrations gradually lowered depthwise from the surface of the epitaxial layer 2E. The impurity concentration of the p-well 6p and the n-well 6n is at 5×10^{15} to 6×10^{16} atoms/cm^3.

5   Subsequently, as shown in Fig. 22, a pad oxide film 12c and the (not-shown) non-oxidizable insulating film of Si_3N_4 are deposited sequentially from the lower layer. After this, the non-oxidizable insulating film is removed from the element separating region but left 10 at the element forming region.

After this, the non-oxidizable insulating film left unremoved is used as a mask to form the field insulating film 3 selectively in the element separating region. After this, as shown in Fig. 23, 15 the element forming region, as enclosed by the field insulating film 3, is formed by the thermal oxidation method with the gate insulating films 4Nc and 4Pc made of SiO_2 having a thickness of about 180 angstroms, for example.

20   Thus in the present embodiment 4, too, the gate insulating films 4Nc and 4Pc are given an excellent film quality by forming them over the epitaxial layer 2E so that their breakdown voltages can be improved. Moreover, the gate insulating films 4Nc and 4Pc can 25 have their defect densities improved by one figure or

more.

Subsequently, the gate insulating films 4Nc and 4Pc are simultaneously formed thereover with the gate electrodes 4Nd and 4Pd made of an n-type poly-silicon

5   of low resistance, for example. After this, these gate electrodes 4Nd and Pd are used as masks to form the paired semiconductor regions 4Na and 4Nb and the paired semiconductor regions 4Pa and 4Pb by the separate ion implantation steps thereby to form the

10   nMOS 4N and pMOS 4P over the epitaxial wafer 2WE.

Here, the gate electrodes 4Nd and 4Pd should not be limited to those made of elemental poly-silicon but can be modified in various manners. For example, the gate electrodes 4Nd and 4Pd may be given the so-called

15   "poly-cide structure", in which a refractory metal silicide film is deposited on poly-silicon of low resistance.

Moreover, the semiconductor region 4Na of the nMOS 4N is formed by doping it with ions of As in a

20   dose of about 1×10^{15} atoms/cm^2, for example. On the other hand, the semiconductor region 4Pa of the pMOS 4P is formed by doping it with ions of BF$_2$ in a dose of about 1×10^{15} atoms/cm^2, for example.

Incidentally, the semiconductor regions 4Na, 4Nb,

25   4Pa and 4Pb may be exemplified by the double diffused

drain structure or the LDD structure, as described above.

After this, as shown in Fig. 24, the insulating film 7 of SiO_2 is deposited on the epitaxial wafer 2WE

5 by the CVD method or the like. This insulating film 7 is mainly composed of the BPSG (i.e., Boro Phospho Silicate Glass) containing B_2O_3 and P_2O_5.

Next, the insulating film 7 is formed with the connection holes 8 for exposing the semiconductor

10 regions 4Na and 4Nb of the nMOS 4N and the semiconductor regions 4Pa and 4Pb of the pMOS 4P to the outside. After this, the conductor film 9 of the Al-Si-Cu alloy, for example, is deposited on the epitaxial wafer 2WE by the sputtering method or the

15 evaporation method.

Subsequently, the conductor film 9 is patterned by the dry etching method or the like to form the electrodes 9Na, 9Nb, 9Pa, 9Pb, 9Sa and 9Sb. After this, the insulating film 7a of SiO_2, for

20 example, is deposited on the epitaxial wafer 2WE by the CVD method of the like. After this, the flattening insulating film 7b of SiO_2 is deposited on the insulating film 7a by the CVD method or the like.

Next, the flattening insulating film 7b is

25 flattened by the CMP (i.e., Chemical Mechanical

Polishing) method or the like.   After this, the

insulating films 7, 7a and 7b are formed with the

connection holes 8a by the dry etching method, as

shown in Fig. 16.

5   Subsequently, the barrier layer 10a1 of TiN, the

conductor layer 10a2 of the $\underline{Al}$ -Si-Cu alloy and the

barrier layer 10a3 of TiN, for example, are deposited

on the epitaxial wafer 2WE sequentially from the lower

layer by the sputtering method or the evaporation

10   method.

Subsequently, those barrier layers 10a1 and 10a3

and conductor layer 10a2 are patterned by the dry

etching method or the like to form the second-layer

wiring line 10a.   After this, the insulating film 7c

15   of SiO_2, for example, is deposited on the epitaxial

wafer 2WE by the CVD method or the like.

After this, the insulating film 11a of SiO_2 is

deposited on the insulating film 7c by the CVD method

or the like.   The insulating film 11b of Si_3N_4 is then

20   deposited on the insulating film 11a by the CVD method

or the like to from the surface protecting film 11.

After this, the individual semiconductor chips

are divided from the epitaxial wafer 2WE to

manufacture the semiconductor integrated circuit

25   device 1, as shown in Fig. 16.

Here, in case the structure of the present

embodiment 4 is applied to a 4M·DRAM (i.e., 4 Megabit

Dynamic RAM), the results of the performances (e.g.,

the gate breakdown voltage) of the gate insulating

5   film are plotted in Fig. 25.

Fig. 25 plots the performances of the gate

insulating film in case the MOS capacitor to have its

gate breakdown voltage evaluated is prepared after the

process for manufacturing the 4M·DRAM is executed to

10   the step of forming the gate insulating film.

It is assumed here that: the gate insulating film

has a thickness of about 18 nm; the gate electrode has

an area of about 4.8 mm^2; and the gate electrode is

made of phosphor-doped poly-silicon.

15   The abscissa indicates the thickness W_E of the

epitaxial layer. On the other hand, the ordinate

indicates the defect density which is calculated from

the following equation by measuring the breakdown

characteristics of about two hundreds of MOS

20   capacitors on the semiconductor wafer (or the

epitaxial wafer) and then by deciding the

non-defective and defective produces according to the

following standards. However, the densities are

generally indicated in relative values with reference

25   to the mirror wafer for the MOS·LSI having no

epitaxial layer.

Standards for Deciding Products Non-Defective in Breakdown Voltage: Electric Field > 10 MV/cm. Here, the electric current is at about 1 mA. For a gate

5   defect density D, the number P of the capacitors measured, and the number N of the defective capacitors, $D = (100/4.8)\ln((P-N)/P)$.

Thanks to the structure of the present embodiment 4, as seen from Fig. 25, it can be confirmed that the

10   defect density can be reduced more by one figure or more than the case, in which the gate insulating film is formed over the mirror wafer, to provide an excellent gate breakdown performance.

As has been described hereinbefore, according to

15   the present embodiment 4, the following effects can be achieved in addition to those of the foregoing embodiment 1.

(1) For manufacturing the semiconductor integrated circuit device, there can be used absolutely the same

20   process as that of the case in which the CMOS circuit is to be formed over the mirror wafer. As a result, the semiconductor integrated circuit device having the CMOS circuit over the epitaxial wafer 2WE can be formed without any change in the design or in the

25   manufacture process.

(2) Since the impurity concentration of the epitaxial layer 2E is made lower than that of the semiconductor substrate body 2S, the resistance of the semiconductor substrate body 2S can be made lower than that of the epitaxial layer 2E to improve the resistance to the latchup.

(Embodiment 5)

Fig. 26(A) is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention.

The semiconductor integrated circuit device 1 of the present embodiment 5, as shown in Fig. 26(A), is exemplified by a 16M·DRAM. Fig. 16(B) is a circuit diagram showing a memory cell of the DRAM. In Fig. 26(A), the lefthand side shows a memory cell region, and the righthand side shows a peripheral circuit region. Incidentally, this peripheral circuit region has the same structure as that of the foregoing embodiment 4, and its description will be omitted.

In the present embodiment 5, too, the impurity concentration of the epitaxial layer 2E is made lower than that of the semiconductor substrate body 2S, as in the foregoing embodiment 4.

As shown in Figs. 26(A) and 26(B), one memory

cell MC is constructed one transfer MOS FET 13 and one capacitor 14.

The transfer MOS·FET 13 is composed of a pair of semiconductor regions 13a and 13b formed in a p-well 6pl, a gate insulating film 13c formed over the epitaxial layer 2E, and a gate electrode 13d formed over the gate insulating film 13c.

Here in the memory cell region, too, the p-well 6pl is formed to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S, as located deeper than the epitaxial layer 2E. Moreover, the impurity concentration of the p-well 6pl is made gradually lower, as in the foregoing embodiment 4, depthwise of the semiconductor substrate 2.

The paired semiconductor regions 13a and 13b are doped with an n-type impurity such as As. In the present embodiment 5, these semiconductor regions 13a and 13b are formed in the epitaxial layer 2E having less defects due to the precipitation of oxygen, so that the junction leakage current can be reduced to improve the performance, reliability and production yield of the DRAM.

With one semiconductor region 13a, there is electrically connected a bit line (BL) 15. This bit

line 15 is composed, for example, of a conductor layer 15a made of polycrystalline silicon of low resistance and a conductor layer 15b formed over the former and made of tungsten silicide or the like.

With the other semiconductor region 13b, on the other hand, there is electrically connected a lower electrode 14a of the capacitor 14. In the present embodiment 5, the semiconductor region 13b is formed in the epitaxial layer 2E having less defects due to the precipitation of oxygen, so that the leakage of the charge accumulated in the capacitor 14 can be suppressed to elongate the charge storage time period thereby to improve the refresh characteristics.

The capacitor 14 is formed into a fin shape and constructed of the lower electrode 14a, an upper electrode 14b, and a (not-shown) insulating film interposed between those electrodes. However, the shape of the capacitor should not be limited to the fin but can be modified in various manners such as a cylindrical shape.

Incidentally, the gate electrode 13d of the transfer MOS FET 13 also acts as the word line (WL). Moreover, reference numerals 16a and 16b appearing in Fig. 26(A) designate channel stopper regions.

Thus in the present embodiment 5, the following

effects can be achieved in addition to those of the foregoing embodiment 1.

Specifically, since the semiconductor region 13b to be electrically connected with the lower electrode 14a of the capacitor 14 is formed in the epitaxial layer 2E, the leakage of the charge accumulated in the capacitor 14 can be suppressed to elongate the charge storage time period thereby to improve the refresh level. As a result, it is possible to improve the performance, reliability and production yield of the DRAM.

(Embodiment 6)

Fig. 27(A) is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention.

The semiconductor integrated circuit device 1 of the present embodiment 6, as shown in Fig. 27(A), is exemplified by a 4M·SRAM (i.e., 4 Megabit Static RAM). In the present embodiment 6, too, the impurity concentration of the epitaxial layer 2E is made lower than that of the semiconductor substrate body 2S, as in the foregoing embodiment 4. Fig. 27(B) is a circuit diagram showing a memory cell of the SRAM.

In the present embodiment 6, as shown in Figs.

27(A) and 27(B), in the semiconductor substrate 2, the

memory cell region is formed with a p-well 6p2, and

the peripheral circuit region is formed with an n-well

6n1.

5   These p-well 6p2 and n-well 6n1 are formed, as in

the foregoing embodiments 4 and 5, to extend from the

surface of the epitaxial layer 2E to the upper portion

of the semiconductor substrate body 2S. Moreover,

their impurity concentrations are made gradually lower   -

10   depthwise of the semiconductor substrate 2 as in the

foregoing embodiment 4.

       The memory cell region is formed with a transfer

MOS·FET 17, a drive MOS·FET 18 and a load MOS FET 19.

       The transfer MOS·FET 17 is composed of: a pair of

15   semiconductor regions 17a and 17b formed in the upper

portion of the p-well 6p2; a gate insulating film 17c

formed over the epitaxial layer 2E; and a gate

electrode 17d formed over the gate insulating film

17c.

20   These semiconductor regions 17a and 17b are doped

with an n-type impurity such as As. One semiconductor

region 17a is electrically connected through the first

-layer wiring line 10 with the bit line 15 (BL and

$\overline{BL}$). The other semiconductor region 17b is

25   electrically connected with a gate electrode 18d of

the drive MOS·FET 18.

Incidentally, the transfer MOS·FET 17 and the drive MOS·FET 18 have their gate electrodes 17d and 18d formed by depositing a refractory metal silicide on the conductor film made of poly-silicon of low resistance, and the transfer MOS·FET 17 has its gate electrode 17d connected with the word line WL.

Moreover, the gate insulating films 17c and 18c are made of SiO_2, for example. Still moreover, the paired semiconductor regions of the drive MOS·FET 18 are positioned in the direction of the channel length of the gate electrode 18d, although not shown.

The load MOS·FET 19 is composed of a gate electrode 19a made of poly-silicon of low resistance, and a pair of semiconductor regions 19c and 19d formed over the gate electrode 19a through a gate insulating film 19b and made of poly-silicon of low resistance. The semiconductor regions 19c and 19d are doped with an n-type impurity such as As.

The peripheral circuit region is formed with the pMOS 4P, for example. This pMOS 4P is composed of: the paired semiconductor regions 4Pa and 4Pb formed in the upper portion of the n-well 6n1; the gate insulating film 4Pc formed over the epitaxial layer 2E; and the gate electrode 4Pd formed over the gate

insulating film 4Pc. These semiconductor region 4Pa and 4Pb are doped with a p-type impurity such as boron.

In the present embodiment 6, the following effects can be achieved in addition to those of the foregoing embodiment 1.

Specifically, according to the structure of the present embodiment 6, the memory cell (MC) of the SRAM is formed over the epitaxial layer 2E having less defects due to the precipitation of oxygen so that the junction leakage current can be reduced in the paired semiconductor regions 17a and 17b of the transfer MOS·FET 17 and the (not-shown) paired semiconductor regions of the drive MOS·FET 18, as composing the memory cell (MC). As a result, the data storage retaining characteristics (e.g., the data retention level) can be improved to reduce the data retention fault percentage. As a result, it is possible to improve the performance, reliability and production yield of the SRAM.

(Embodiment 7)

Fig. 28 is a section showing an essential portion of a semiconductor integrated circuit device according to another embodiment of the present invention.

The semiconductor integrated circuit device 1 of

the present embodiment 7, as shown in Fig. 28, is

exemplified by a flash memory (i.e., flash EEPROM

(Electrically Erasable Programmable ROM)) capable of

5   electrically erasing/programming data. In the present

embodiment 7, too, as in the foregoing embodiment 4,

the impurity concentration of the epitaxial layer 2E

is made lower than that of the semiconductor substrate

body 2S.

10   In the present embodiment 7, too, the

semiconductor substrate 2 is formed thereover with a

p-well 6p3 and an n-well 6n2. These p-well 6p3 and

n-well 6n2 are formed, as in the foregoing embodiments

4 to 6, to extend from the surface of the epitaxial

15   layer 2E to the upper portion of the semiconductor

substrate body 2S. Moreover, their impurity

concentrations are made gradually deeper depthwise of

the semiconductor region 2, as in the foregoing

embodiment 4.

20   The memory cell region is formed with a memory

cell MC1. This memory cell MC1 is constructed of a

single MOS·FET. The memory cell MC1 is composed of: a

pair of semiconductor regions 20a and 20b formed in

the upper portion of the p-well 6p3; a gate insulating

25   film 20c formed over the epitaxial layer 2E; a

floating gate electrode 20d formed over the gate

insulating film 20c; a control gate electrode 20e

formed over the floating gate electrode 20d through

the (not-shown) insulating film.

5   One semiconductor region 20a is composed of a

semiconductor region 20a1 and a semiconductor region

20a2 formed in the former. The semiconductor region

20a1 is doped with an n^--type impurity such as

phosphor, and the semiconductor region 20a2 is doped

10   with an n^+-type impurity such as As.

Moreover, the other semiconductor region 20b is

composed of a semiconductor region 20b1 and a

semiconductor region 20b2 formed in the former. The

semiconductor region 20b1 is doped with a p^+-type

15   impurity such as boron, and the semiconductor region

20b2 is doped with an n^+-type impurity such as As.

On the other hand, the peripheral circuit region

is formed with the nMOS 4N and the pMOS 4P, for

example. The nMOS 4N is composed of: the paired

20   semiconductor regions 4Na and 4Nb formed in the upper

portion of the p-well 6p3; the gate insulating film

4Nc formed over the epitaxial layer 2E; and the gate

electrode 4Nd formed over the gate insulating film

4Nc. These semiconductor regions 4Na and 4Nb are

25   doped with an n-type impurity such as phosphor.

The pMOS 4P is composed of: the paired
semiconductor regions 4Pa and 4Pb formed in the upper
portion of the n-well 6n2; the gate insulating film
4Pc formed over the epitaxial layer 2E; and the gate
5   electrode 4Pd formed over the gate insulating film
4Pc.   These semiconductor regions 4Pa and 4Pb are
doped with a p- type impurity such as boron.

The semiconductor region 4Na of the nMOS 4N and
the semiconductor region 4Pa of the pMOS 4P are
10   electrically connected through the first-layer wiring
line 10 to construct the CMOS circuit.

Thus in the present embodiment 7, the following
effects can be achieved in addition to those of the
foregoing embodiment 1.

15   Specifically, in the structure of the present
embodiment 7, the memory cell of the flash memory
(i.e., EEPROM) is formed over the epitaxial layer 2E
having less defects such as the precipitation of
oxygen, so that the breakdown voltage of the gate
20   insulating film 20c can be raised to improve the data
programming resistance. Moreover, the erasure
dispersion at the time of erasing the data can be
reduced. As a result, it is possible to improve the
performance, reliability and production yield of the
25   flash memory (i.e., EEPROM).

Although our invention has been specifically

described in connection with its embodiments, it

should not be limited to its foregoing embodiments 1

to 7 but can naturally be modified in various manners

5   without departing the gist thereof.

For example, the foregoing embodiments 1 to 3

have been described in case the gettering layer is

made of poly-silicon. However, the present invention

should not be limited thereto but can be modified in   −

10   various manners. For example, the gettering layer may

be formed by the method of mechanically forming a

working strain on the back of the semiconductor

substrate body, the method of properly adjusting or

precipitating the oxygen element which is present in

15   the semiconductor substrate body, or the method of

doping the semiconductor substrate with carbon ions.

Alternatively, the structure may be dispensed with the

gettering layer. In the method of properly adjusting

or precipitating the oxygen element in the

20   aforementioned semiconductor substrate body, the

substrate gettering effect can be enhanced by setting

the oxygen concentration to about or more than 9×10^{17}

atoms/cm^3. At the same time, the gate insulating film

can be formed over the epitaxial layer formed over the

25   semiconductor substrate body and containing no oxygen

element, thereby to improve the breakdown

characteristics of the gate insulating film.

Specifically in the prior art for forming the gate

insulating film directly over the principal surface of

5   the semiconductor substrate body, if the oxygen

concentration present in the semiconductor substrate

body is made as high as 9×10^{17} atoms/cm^3, the oxygen

is precipitated in the aforementioned principal

surface so that any clean gate insulating film is not

10   formed to deteriorate the breakdown characteristics of

the gate insulating film. In the prior art,

therefore, the oxygen concentration has to be lowered

to make the gettering effect insufficient.

Moreover, the foregoing embodiments 1 to 7 have

15   been described in case the epitaxial layer is formed

by the epitaxial growth method using the SiH$_4$ gas.

However, the present invention should not be limited

thereto but can be modified in various manners. For

example, the epitaxial layer may be formed by the

20   epitaxial growth method using silicon tetrachloride

(SiC$\underline{1}_4$) gas.

Moreover, the foregoing embodiments 1, 2 and 4 to

7 have been described in case the semiconductor

substrate body and the epitaxial layer are made of p$^-$-

25   type Si. However, the present invention should not be

limited thereto but can be modified such that the
semiconductor substrate body and the epitaxial layer
are made of n⁻-type Si. In the foregoing embodiment 3,
moreover, the semiconductor substrate body and the

5   epitaxial layer may be made of n⁻-type Si, and the p⁺-
type semiconductor region may be made of n⁺-type Si.

Moreover, the foregoing embodiment 3 has been
described in case the p⁺-type semiconductor region for
suppressing the latchup is formed all over the

10   semiconductor substrate body. However, the present
invention should not be limited thereto but can be
modified in various manners. For example, a p⁺-type
semiconductor region may be formed below the CMOS
circuit forming region.

15   Moreover, the foregoing embodiment 3 has been
described in case the p⁺-type semiconductor region is
formed at a predetermined depth from the principal
surface of the semiconductor substrate body. However,
the present invention should not be limited thereto

20   but may be modified such that the p⁺-type semiconductor
region 2B is formed over the principal surface of the
semiconductor substrate body 2S, as shown in Fig. 29.
Incidentally, Fig. 30 shows the case in which the
epitaxial layer 2E is formed over the semiconductor

25   substrate body 2S of Fig. 29.

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In the semiconductor integrated circuit device having the structure described in the foregoing embodiment 3, moreover, the non-defective layer of the semiconductor integrated circuit device of the foregoing embodiment 2 may be formed below the epitaxial layer.

Moreover, the techniques having been described in connection with the foregoing embodiments 1 to 3 can also be applied to another semiconductor integrated circuit device such as the semiconductor integrated circuit device which has a semiconductor memory circuit such as the flash memory represented by the DRAM, the SRAM or the ROM (Read Only Memory).

Moreover, the techniques of the foregoing embodiments 1 to 7 can also be applied to the semiconductor integrated circuit device which has a logic circuit such as the so-called "microcomputer".

Moreover, the semiconductor substrate body 2S having a size as large as 12 inches may be useful.

In the description thus far made, our invention has been described in case it is applied to the semiconductor integrated circuit device having the CMOS circuit having the field of application of its background. However, the present invention should not be limited thereto but can be modified in various

manners. For example, the present invention can be applied to another semiconductor integrated circuit device such as the semiconductor integrated circuit device having the bipolar transistors or the

5   semiconductor integrated circuit device having a BiCMOS circuit composed of the bipolar transistors and the CMOS circuit. In the description thus far made, moreover, the MOS·FET is used, but the present invention should not be limited thereto. For example,

10   the MIS·FET (i.e., Metal-Insulator-Semiconductor·FET), which has its gate insulating film formed of the semiconductor single crystal layer (or epitaxial layer) 2E of thermally oxidized SiO_2 and the silicon nitride film (SiN) formed over the SiO_2.

15   The effects to be obtained by the representative of the invention disclosed herein will be briefly described in the following.

(1) According to the semiconductor wafer manufacturing process of the present invention, any

20   semiconductor substrate body of high price and density need not be used so that the cost for the semiconductor wafer capable of realizing high element characteristics and reliability can be lowered.

(2) According to the semiconductor integrated circuit

25   device manufacturing process of the present invention,

a gate insulating film having an excellent film
quality can be formed by forming the gate insulating
film of a MOS·FET over a semiconductor single crystal
layer so that the gate insulating film can have its

5   breakdown voltage raised to reduce the defect density
of the gate insulating film. Moreover, the
semiconductor substrate body of high price and density
need not be used, but the semiconductor single crystal
layer can be thinned to reduce the cost for the

10   semiconductor integrated circuit device having high
element characteristics and reliability. As a result,
it is possible to improve the performance, production
yield and reliability of the semiconductor integrated
circuit device and to lower the cost for the

15   semiconductor integrated circuit device.

(3)   According to the semiconductor integrated circuit
device manufacturing process of the present invention,
the degree of freedom for setting the impurity
concentration and depth is so high when a

20   semiconductor region such as a well is formed in the
semiconductor substrate, as to facilitate the control
of the formation. As a result, it is possible to
reduce the defective products thereby to improve the
production yield. Moreover, the cost for the

25   semiconductor integrated circuit device can be

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lowered.

(4) According to the semiconductor integrated circuit device manufacturing process of the present invention, the impurity concentration of the semiconductor substrate body is made higher than that of the semiconductor single crystal layer, so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup. As a result, it is possible to further improve the performance, production yield and reliability of the semiconductor integrated circuit device.

(5) According to the semiconductor integrated circuit device manufacturing process of the present invention, since the first semiconductor region is formed by the ion implantation method and the thermal diffusion method, the semiconductor integrated circuit device can be manufactured without being accompanied by any change in the design or manufacture process but by using the same method as that of the semiconductor integrated circuit device having the so-called "mirror wafer", when it is to be manufactured by using the semiconductor wafer having the semiconductor single crystal layer over the semiconductor substrate body.

(6) According to the semiconductor integrated circuit

device manufacturing process of the present invention, since the memory cell of the dynamic type random access memory is formed over the semiconductor single crystal layer having less defects such as the

5   precipitation of oxygen, it is possible to reduce the junction leakage current in the source region and the drain region of the transfer MOS·FET of the memory cell. Since, moreover, the charge leakage in the capacitor of the memory cell can be suppressed to

10   elongate the charge storage time period, it is possible to improve the refresh characteristics. As a result, it is possible to improve the performance, reliability and production yield of the dynamic type random access memory.

15   (7)   According to the semiconductor integrated circuit device manufacturing process of the present invention, since the memory cell of the static type random access memory is formed over the semiconductor single crystal layer having less defects such as the

20   precipitation of oxygen, the junction leakage current of the source region and drain region of the MOS·FET composing the memory cell can be reduced to improve the data storage retaining characteristics (e.g., the data retention level) thereby to reduce the data

25   retention fault percentage. As a result, it is

possible to improve the performance, reliability and production yield of the static type random access memory.

(8) According to the semiconductor integrated circuit device manufacturing process of the present invention, the memory cell of a read only memory capable of electrically erasing and programming data is formed over the semiconductor single crystal layer having less defects such as the precipitation of oxygen, so that the resistance to the data programming can be improved. Moreover, the dispersion of the data erasure can be reduced. As a result, it is possible to improve the performance, reliability and production yield of the read only memory capable of electrically erasing and programming the data.